In the Claims:

1. (Currently amended) A content addressable memory (CAM) device, comprising:

a priority resolution circuit ~~that is~~ configured to hierarchically resolve competing soft priorities between a plurality of active hit signals according to numeric significance so that a first of the plurality of active hit signals having a first soft priority will block resolution of a second of the plurality of active hit signals having a second priority when the first priority is higher than the second priority and vice versa when the second priority is higher than the first priority.

2. (Original) The CAM device of Claim 1, wherein said priority resolution circuit is configured to resolve competing hard priorities between two or more of the plurality of active hit signals having equivalent highest soft priorities by identifying which of the two or more of the plurality of active hits signals has the highest hard priority.

3. (Original) The CAM device of Claim 2, wherein said priority resolution circuit comprises a MSB soft priority resolution stage and a LSB soft priority resolution stage.

4. (Currently amended) The CAM device of Claim 3, wherein said priority resolution circuit comprises a hard priority resolution stage ~~that is~~ electrically coupled to outputs of said LSB soft priority resolution stage; and wherein said priority resolution circuit is further configured so that competing and unequal soft priorities of at least some of the plurality of active hit signals are completely resolved by the MSB and LSB soft priority resolution stages prior to further resolution of hard priority by the hard priority resolution stage.

5. (Currently amended) The CAM device of Claim 1, further comprising:

a plurality of CAM array blocks having respective soft priorities assigned thereto; **[[and]]**

wherein said priority resolution circuit comprises a plurality of registers that retain the soft priorities assigned to said plurality of CAM array blocks; and

wherein said priority resolution circuit is configured so that the soft priorities retained by the plurality of registers can be arranged in any order regardless of the values of hard priorities assigned to said plurality of CAM array blocks.

6. (Currently amended) A content addressable memory (CAM) device, comprising:

a plurality of CAM array blocks having respective soft priorities assigned thereto; and

a hierarchical priority resolution circuit ~~that is~~ configured to identify a highest priority one of said plurality of CAM array blocks having respective matching entries therein during a search operation, by evaluating the soft priorities of said plurality of CAM array blocks according to numeric significance so that matching entries in a first of said plurality of CAM array blocks are treated as having higher priority than matching entries in a second of said plurality of CAM array blocks when the soft priority of the first of said plurality of CAM array blocks is higher than the soft priority of the second of said plurality of CAM array blocks and vice versa when the soft priority of the second of said plurality of CAM array blocks is higher than the soft priority of the first of said plurality of CAM array blocks.

7. (Original) The CAM device of Claim 6, wherein said hierarchical priority resolution circuit is configured to sequentially evaluate the soft priorities of said plurality of CAM array blocks in descending order according to numeric significance.

8. (Currently amended) The CAM device of Claim 6, wherein said hierarchical priority resolution circuit comprises a plurality of programmable registers that retain the soft priorities; and wherein said hierarchical priority resolution circuit is configured so that the soft priorities retained by the plurality of programmable registers can be arranged in any order regardless of the values of hard priorities assigned to said plurality of CAM array blocks.

9. (Original) The CAM device of Claim 6, wherein said hierarchical priority resolution circuit comprises:

a first soft priority resolution circuit that is electrically coupled in a wired-OR manner to a first plurality of signal lines; and

a second soft priority resolution circuit that is electrically coupled in a wired-OR manner to a second plurality of signal lines.

10. (Original) The CAM device of Claim 9, wherein the first and second plurality of signal lines are floated or biased at precharged levels during the search operation.

11. (Original) The CAM device of Claim 9, wherein said hierarchical priority resolution circuit further comprises:

a third soft priority resolution circuit that is electrically coupled in a wired-OR manner to a third plurality of signal lines.

12. (Original) The CAM device of Claim 11, wherein said hierarchical priority resolution circuit further comprises:

a hard priority resolution circuit that is electrically coupled to outputs of said third soft priority resolution circuit.

13. (Original) The CAM device of Claim 6, wherein said hierarchical priority resolution circuit comprises:

a soft priority resolution circuit; and

a hard priority resolution circuit that is electrically coupled to outputs of said soft priority resolution circuit.

14. (Original) The CAM device of Claim 6, wherein said hierarchical priority resolution circuit comprises:

a soft priority resolution circuit that is electrically coupled in a wired-OR manner to a first plurality of signal lines that are floated or biased at precharged levels during a priority resolution operation; and

a hard priority resolution circuit that is electrically coupled to outputs of said soft priority resolution circuit.

15. (Currently amended) A content addressable memory (CAM) device, comprising:

a priority resolution circuit ~~that is~~ configured to resolve competing soft priorities between a plurality of active hit signals associated with a respective plurality of CAM array blocks, said priority resolution circuit further configured to support all orders of priority between the plurality of CAM array blocks so that a first of the plurality of active hit signals having a first soft priority will block resolution of a second of the plurality of active hit signals having a second priority when the first priority is higher than the second priority and vice versa when the second priority is higher than the first priority.

16. (Currently amended) The CAM device of Claim 15, wherein said priority resolution circuit is configured to resolve competing hard priorities between at least two of the active hit signals having the same soft priority, subsequent to fully resolving competing soft priorities between other ones of the plurality of active hit signals having unequal soft priorities.

17. (Original) The CAM device of Claim 16, wherein said priority resolution circuit is a hierarchical priority resolution circuit having at least a MSB soft priority resolution stage and a LSB soft priority resolution stage.

18. (Original) The CAM device of Claim 17, wherein said priority resolution circuit comprises a hard priority resolution stage that is electrically coupled to outputs of said LSB soft priority resolution stage.

19. (Currently amended) A content addressable memory (CAM) device, comprising:

a priority resolution circuit ~~that is~~ configured to resolve competing soft priorities between a plurality of active hit signals associated with a corresponding plurality of CAM array blocks in order to identify two or more active hit signals having highest equivalent soft priorities and [[is]] further configured to resolve competing hard priorities between the two or more active hit signals in order to identify one as having the highest hard priority; and

wherein said priority resolution circuit is configured to resolve the competing soft priorities for all possible combinations of soft priority order between the plurality of active hit signals.

20. (Original) The CAM device of Claim 19, wherein the competing soft priorities of the plurality of active hit signals are resolved by evaluating the soft priorities in a MSB to LSB sequence.

21. (Original) The CAM device of Claim 19, wherein said priority resolution circuit is a hierarchical priority resolution circuit having at least two soft priority resolution stages and a hard priority resolution stage.

22. (Currently amended) A content addressable memory (CAM) device, comprising:

a plurality of CAM array blocks having respective soft priorities assigned thereto; and

means for identifying a highest priority one of said plurality of CAM array blocks having respective matching entries therein during a search operation, by evaluating the soft priorities of said plurality of CAM array blocks according to numeric significance so that matching entries in a first of said plurality of CAM array blocks are treated as having higher priority than matching entries in a second of said plurality of CAM array blocks when the soft priority of the first of said plurality of CAM array blocks is higher than the soft priority of the second of said plurality of CAM array blocks and vice versa when the soft priority of the second of said plurality of CAM array blocks is higher than the soft priority of the first of said plurality of CAM array blocks.

23. (Currently amended) A content addressable memory (CAM) device, comprising:

a hierarchical priority resolution circuit ~~that is~~ configured to identify a highest priority one of a plurality of CAM array blocks having respective matching entries therein during a search operation by:

evaluating soft priorities of the plurality of CAM array blocks according to numeric significance so that matching entries in a first of said plurality of CAM array blocks are treated as having higher priority than matching entries in a second of said plurality of CAM array blocks when the soft priority of the first of said plurality of CAM array blocks is higher than the soft priority of the second of said plurality of CAM array blocks and vice versa when the soft priority of the second of said plurality of CAM array blocks is higher than the soft priority of the first of said plurality of CAM array blocks; and then

after completion of said evaluating soft priorities, evaluating competing hard priorities between at least two of the plurality of CAM array blocks having the same soft priorities.

24. (Currently amended) A content addressable memory (CAM) device, comprising:

a plurality of CAM array blocks that each have respective soft and hard priorities assigned thereto; and

a priority resolution circuit ~~that is~~ configured to resolve competing soft priorities for all possible combinations of soft priority order between said plurality of CAM array blocks and further configured to resolve ~~identify a highest priority one of said plurality of CAM array blocks having respective matching entries therein during a search operation by resolving~~ competing hard priorities between at least two of said plurality of CAM array blocks having the same soft priority, during an operation to search the plurality of CAM array blocks to identify respective matching entries therein.

25. (Original) The CAM device of Claim 24, wherein the CAM device comprises 2^{N+1} CAM array blocks therein, where N is an integer; and wherein said priority resolution circuit comprises $\log_2 N$ groups of precharged signal lines that are used during a priority resolution operation to resolve competing soft priorities between hit signals generated by said plurality of CAM array blocks.

26. (Original) The CAM device of Claim 24, wherein the CAM device comprises 2^{N+1} CAM array blocks, where N is an integer; and wherein said priority resolution circuit comprises $\log_2 N$ groups of N or N-1 precharged signal lines.

27. (Original) The CAM device of Claim 24, wherein the CAM device comprises $(2^x)^y$ CAM array blocks, where x and y are integers; and wherein said priority resolution circuit comprises y groups of precharged signal lines having 2^x or 2^x-1 signal lines per group.

28. (Original) The CAM device of Claim 27, wherein x and y represent a pair of integers selected from the pair groups (x,y) consisting of (3,3), (2,4) and (3,2).

Claim 29 (Canceled).

30. (Currently amended) A content addressable memory (CAM) device, comprising:

a plurality of CAM array blocks that ~~each have~~ having respective soft priorities associated therewith that are programmable and respective hard priorities associated therewith that are fixed according to layout position; and

a soft priority resolution circuit ~~that is~~ configured to process first and second active hit signals generated by first and second CAM array blocks within said plurality of CAM array blocks during a search operation, respectively, using wired-OR logic to identify a highest priority one of the first and second active hit signals and selectively block another one of the first and second active hit signals from being further processed as a highest priority candidate;

wherein said wired-OR logic is configured to support all possible combinations of soft priority order between said plurality of CAM array blocks.

Claims 31-45 (Canceled).

46. (Currently amended) A content addressable memory (CAM) device, comprising:

$(2^x)^y$ CAM array blocks; and

a soft priority resolution circuit that hierarchically resolves competing soft priorities between a plurality of active hit signals generated by a plurality of the CAM array blocks during a search operation and comprises y groups of precharged signal lines having 2^x or 2^x-1 signal lines per group that support soft priority resolution of all possible combinations of soft priority order between the plurality of active hit signals.

47. (Original) The CAM device of Claim 46, wherein x and y represent a pair of integers selected from the pair groups (x,y) consisting of (3,3), (2,4) and (3,2).

Claims 48-58 (Canceled).